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Analysis of Low Power ADC based Receiver Architectures

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ABSTRACT

A common trend in digital communications has been the increasing use of digital signal processing especially with CMOS technology. The realization of multi-GSample/s (GS/s) analog-to-digital converters (ADCs) draws a growing interest in incorporating CMOS ADCs as the frontend of high-speed serializers/deserializers (SerDes). Digital receiver frontends have emerged as a possible solution for the next-generation serial I/O receiver design in advanced CMOS technologies. Power dissipation has become an important consideration both due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated applications like mobile, PDA's and laptops etc. Today's technology has been changing rapidly to meet these requirements. This paper outlooks the different design architectures used to address the above issues to meet the wide spread requirements of high speed and low power ADC based serial I/O receivers.

I.INTRODUCTION

DATA RATES FOR serial I/O links have been steadily increasing with on-chip processing rates and logic density. In order to utilize a limited number of I/O pins, the signaling rates per lane have exceeded 10 Gbits per second (Gb/s). Serial I/O designs have to achieve low bit error rates (BER) in the presence of link nonidealities such as channel loss, reflection caused by impedance discontinuity and the crosstalk and constrained by a stringent power budget.

To effectively meet these challenges, the common receiver design has used continuous- time or discrete-time forward (FFE) and feedback (DFE) [1]–[4] equalizers such as one shown in Fig.A common trend in digital communications has been the increasing use of digital signal processing especially with CMOS technology.

The realization of multi-GSample/s (GS/s) analog-to-digital converters (ADCs) draws a growing interest in incorporating CMOS ADCs as the frontend of high-speed serializers/deserializers

(SerDes) [5], [6] and electronic dispersion compensation (EDC) of optical links [6], [7].Compared with traditionalmixed- mode approach, the advantages of such ADC-based receiver include:1) better programmability and extensibility to different channel characteristics; 2) better equalization robustness to process and coefficient variations; 3) possibility of using more powerful signal processing techniques such as sequence detection to achieve lower BER; and 4)
potential of adopting complex modulation schemes beyond binary PAM.

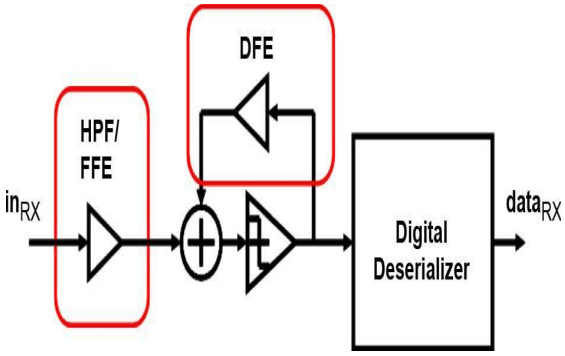

Fig. 1. Mixed-mode SerDes receiver with FFE and DFE. The feedforward filter may also incorporate a high-pass filter (HPF). The implementation may also be split between the transmitter and receiver.

II-ADC-Based Serial I/O Receivers

Despite the advantages of an ADC-based receiver, power consumption and complexity (multibit ADC and digital equalization) impose a limit to its application [8]. The fully digital signal recovery is prevailing in several wired data links such as DSL (< 100Mb/s per channel) [9], [10], PRML read channel (< 1Gb/s per channel) [11], [12] and copper Ethernet (<3Gb/s per channel) [13], [14] to address the complex channel characteristic by higher utilization of the channel capacity.However, the analog (continuous-time high-pass filter) or mixed-mode (FFE/DFE) equalization approach still dominates in the low-attenuating chip-to-chip communication due to the simplicity and low power consumption.

On the other hand, in the high data rate application such as backplane with high attenuation (< 20dB) or multimode optical link environment, ADC-based receiver [5] has shown sufficiently comparable power/performance to be considered in lieu of the traditional mixed-mode approach [15], [16]. As shown in a basic digital receiver comprises an ADC to digitize the received signal and a digital processor to perform channel equalization, data detection, and clock recovery.

An optional analog front-end can be used to buffer the signal and provide some equalization. This paper presents an ADC-based receiver that uses a low-gain analog and mixed-mode pre-equalizer in conjunction with non-uniform reference levels for the ADC. The combination compensates for both the frontend non- ideality and the channel response while maintaining low ADC resolution and hence enables low power consumption. The diagram of the AFE in our proposed ADC-based receiver is shown in Fig. 3, which comprises a continuous-time HPF, a sampled-FIR, and a VGA to perform receiver pre-filtering.

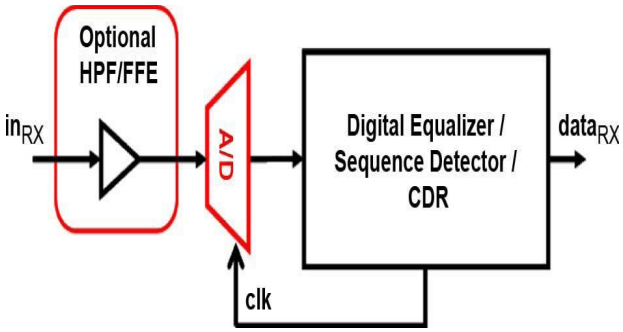

Fig. 2. Generic ADC-based receiver architecture.

The low-gain AFE dramatically reduces the requirement of ADC and digital post processing, and also allows scalability for both data rate and technology.

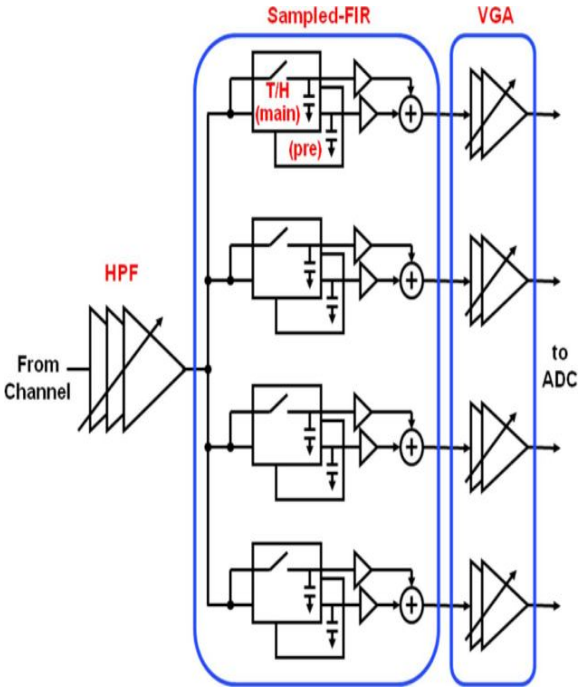

Fig. 3. Block diagram of the AFE in the proposed ADC-based receiver. It consists of a continuous-time HPF, a pre-tap sampled-FIR, and a VGA for receiver pre-filtering

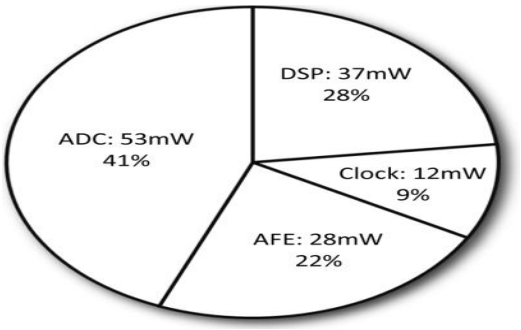

Fig. 4.Receiver power breakdown.

The power breakdown is shown in Fig. 4. It is noteworthy that the sum of ADC and DSP power are almost 70% of total power and they are both expected to be reduced with the technology scaling.

III - Low-Power Highly Digitized Receiver For GFSK Applications

This architecture describes the design and measurement results of a low-power highly digitized receiver for Gaussian frequency-shift keying modulated input signals at 2.4 GHz.

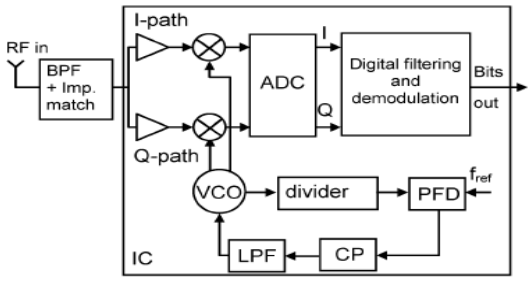

Fig. 5. Simplified block diagram of the receiver.

A simplified block diagram of the receiver is shown in Fig. 5. An external bandpass filter (BPF) selects the 2.4-GHz band and performs impedance matching [17]. Two matched low- noise amplifiers (LNAs) are used in parallel to provide sufficient isolation between the in-phase (I) and quadrature (Q) channels after the mixers. The LNAs have been implemented as V–I converters. The RF output current is down-converted to a low IF of 500 kHz by passive mixers, driven directly by a quadrature voltage-controlled oscillator (VCO) in a PLL. The measured power consumptions of the various blocks in the receiver chain are listed in Table I. The supply voltage for the analog part is 1.8 V, whereas the digital supply voltage is 1.4 V. The total power consumption is 31.7 mW in co

TABLE-1
MEASURED POWER CONSUMPTION OF RECEIVER BLOCKS

Block	Power consumption
2xLNA	2x0.3 mAx1.8 V=1.1 mW
PLL	7.6 mAx1.8 V=13.7 mW
ADC	2.3 mAx1.8 V=4.1 mW
Bandgap	0.1 mAx1.8 V=0.2 mW
Crystal oscillator	1.2 mAx1.8 V=2.2 mW
Digital filter+demodulator	7.4 mAx1.4 V=10.4 mW
Total (analog+digital)	31.7 mW

IV- Variable Reference ADC

The receiver architecture is shown in Fig.1, which consists of an analog/mixed-mode frontend (AFE), a 4-way interleaved ADC, and a digital equalizer. In the AFE, a HPF, a sampled pre-tap FIR, and a VGA have been built to explore various pre-shaping [18]. While the HPF provides a low-power prefiltering for post-cursor ISI, the FIR can cancel the non- causal pre-cursor ISI which is critical in high-attenuation channel. A VGA (up to 10dB) buffers the signal before the ADC and provides an alternative for ADC FSR

adjustment [19][20]. The ADC has variable references with up to 4-bit or 16-comparators. The reference voltage of each comparator can be adjusted by coarse tuning (selecting the tap-point from the resistor ladder) and fine tuning (controlling the PMOS body bias of the reference buffers) (Fig. 1). By combining both methods, the reference tuning range of each comparator is more than 100mV with 2mV step size, which is sufficient to provide the offset cancellation of a 4-bit ADC, and also enables the variable reference tuning.

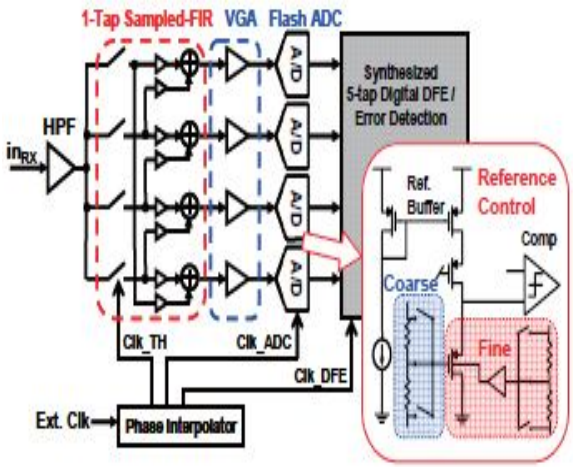

Fig. 6. Receiver architecture.

The receiver consumes 130mW in 1.1V supply. The power breakdown is 28mW for the AFE (with T/H), 53mW for 16- comparator ADC (with clock buffer and reference generator),12Mw of clock interpolation/buffering, and 37mW of digital DFE. The total power efficiency is 13pJ/bit.

V- Embedded Equalization for ADC Based Serial I/O Receivers

A hybrid ADC receiver architecture which includes embedded equalization and selective digital equalization power-down based on threshold detection is proposed. [21].

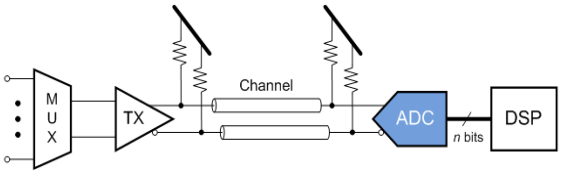

Fig. 7. High speed serial I/O link with ADC-based receiver

CMOS technology scaling allows for the efficient implementation of powerful on-chip digital signal processing (DSP) algorithms for equalization and symbol detection. This motivates the use of Analog to digital converter (ADC)-based analog front ends in I/O receiver design [22], as shown in Fig Here, the incoming data is quantized, allowing the ISI cancellation to be implemented in the digital domain. This digital equalization offers robustness to PVT variations and is easier to re-configure than mixed-signal equalization circuitry. Moreover, an ADC-based receiver also allows for more spectrally-efficient modulation schemes such as duobinary or PAM4, and more complicated equalization methods such as sequence estimation.

Despite these advantages, ADC-based receivers are generally more complex and consume higher power than binary receivers. Even with state of the art multi- GS/s ADC implementations [23], power is often prohibitive for many systems where link power efficiency is the key metric. The digital equalization that follows the ADC can also consume significant power, comparable to the power of the ADC [22].

The proposed hybrid ADC receiver architecture is shown in Fig. 8. Any samples which are below the necessary performance threshold level, as indicated by the threshold detector, are passed through the digital equalizer, while samples which exceed the threshold are treated as reliable decisions. For systems with embedded DFE, the effect of DFE subtraction is reversed in the digital domain in order to not limit the BER performance. The performance of the proposed architecture in terms of potential power savings of digital equalization is shown in Fig. 9. The percentage of digital equalization power saving is given by the probability that the output exceeds the BER=10^{-12} threshold value, quantized to the minimum ADC resolution. With embedded FFE equalization, saving of more than 50% of digital equalization power is possible for up to 37dB of attenuation at Nyquist frequency.

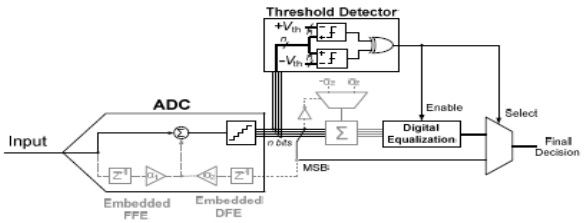

Fig 8. Hybrid ADC architecture with modified threshold.

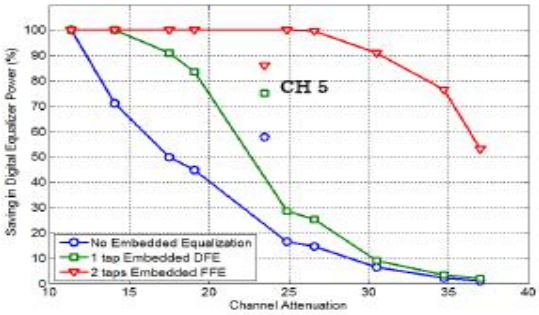

Fig. 9. Potential digital power savings with proposed
hybrid-ADC receiver architecture.

VI. CONCLUSION

Today technology has been changing rapidly to meet requirements like speed, area and power. ADC-based serial I/O receiver draws growing interest with technology scaling. Power consumption remains among the key issues for both the high-speed ADC and the high-throughput DSP. Paper is explored for the different architectures to address power and speed related issues. The first architecture shows that many ADC specifications such as resolution can be relaxed leading to power savings. At the same time, noise and offset specification for a SerDes ADC is often more stringent than a general purpose ADC.

The paper also shows a substantial power trade-off by reducing the amount of digital signal processing through incorporating and jointly-optimizing low-gain mixed-signal/analog prefiltering. In the second architecture the receiver has been realized in a standard 0.18- m CMOS process and measures 3.5 mm2. The only external components are an antenna filter and a crystal. The power consumption is only 32 mW in the continuous mode, which is at least a factor of two lower than state-of-the-art CMOS receivers.

Third paper shows power-performance improvements by incorporating and jointly-optimizing the low-gain pre-filtering in an AFE and variable reference voltages for the ADC comparators. The receiver consumes 130mW in 1.1V supply. The power breakdown is 28mW for the AFE (with T/H), 53mW for 16-comparator ADC (with clock buffer and reference generator), 12mW of clock interpolation/buffering, and 37mW of digital DFE. The total power efficiency is 13pJ/bit.

In fourth architecture, performance of ADC-based analog front-ends with embedded equalization was evaluated. It was shown that embedded FFE results in savings of ADC resolution and that embedded DFE can also provide improved BER performance.

A new hybrid ADC receiver architecture is proposed which employs embedded equalization and a reliable decision threshold for enabling additional digital equalization. By enabling the digital equalizer only when necessary, this architecture is capable of achieving more than 50% of potential savings in digital equalization power.

Thus the study shows the overall power can be improved by suitably designing low gain filter, AFE and variable reference ADC's with embedded equilization. Further improvement in power can be achieved by highly digitized ADC based receiver designs.

REFERENCES

[1] V. Balan, J. Caroselli, J.-G. Chern, C. Chow, R. Dadi, C. Desai, L. Fang, D. Hsu, P. Joshi, H. Kimura, C. Y. Liu, T.-W. Pan, R. Park, C. You, Y. Zeng, E. Zhang, and F. Zhong, "A 4.8–6.4-Gb/s serial link for backplane applications using decision feedback equalization," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1957–1967, Sep. 2005.

[2] K.-L. J. Wong, A. Rylyakov, and C.-K. K. Yang, "A 5-mW 6-Gb/s quarter-rate sampling receiver with a 2-Tap DFE using soft decisions," *IEEE J. Solid-State Circuits* vol. 42, no. 4, pp. 881–888, Apr. 2007.

[3] Y.-S. Sohn, S.-J. Bae, H.-J. Park, C.-H. Kim, and S.-I. Cho, "A 2.2 Gbps CMOS look-ahead DFE receiver for multidrop channel with pin-to-pin time skew compensation," in *Proc. IEEE Custom Integr.Circuits Conf.*, 2003, pp. 473–476.

[4] V. Stojanovic, A. Ho, B. Garlepp, F. Chen, J.Wei, E. Alon, C.Werner, J. Zerbe, and M. A. Horowitz, "Adaptive equalization and data recovery in a dual-mode (PAM2/4) serial link transceiver," in *VLSI Circuits Symp. Dig. Tech. Papers*, 2004, pp. 348–351.

[5] M. Harwood, N. Warke, R. Simpson, T. Leslie, A. Amerasekera, S. Batty, D. Colman, E. Carr, V.

Gopinathan, S. Hubbins, P. Hunt, A. Joy, P. Khandelwal, B. Killips, T. Krause, S. Lytollis, A. Pickering, M. Saxton, D. Sebastio, G. Swanson, A. Szczepanek, T.Ward, J.Williams, R. Williams, and T. Willwerth, "A 12.5 Gb/s SerDes in 65 nm CMOS using a baud-rate ADC with digital receiver equalization and clock recovery," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf. (ISSCC 2007)*, pp. 436–591.

[6] J. Cao, B. Zhang, U. Singh, D. Cui, A. Vasani, A. Garg, W. Zhang, N. Kocaman, D. Pi, B. Raghavan, H. Pan, I. Fujimori, and A. Momtaz, "A 500 mW digitally calibrated AFE in 65 nm CMOS for 10 Gb/s serial links over backplane and multimode fiber," in *Dig. Tech. Papers IEEE Solid-State Circuits Int. Conf. (ISSCC 2009)*, pp. 370–371.

[7] O. E. Agazzi, M. R. Hueda, D. E. Crivelli, H. S. Carrer, A. Nazemi, G. Luna, F. Ramos, R. Lopez, C. Grace, B. Kobeissy, C. Abidin, M. Kazemi, M. Kargar, C. Marquez, S. Ramprasad, F. Bollo, V. Posse, S. Wang, G. Asmanis, G. Eaton, N. Swenson, T. Lindsay, and P. Voois, "A 90 nm CMOSDSP MLSD transceiver with integrated AFE for electronic dispersion compensation of multimode optical fibers at 10 Gb/s," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2939–2957, Dec. 2008.

[8] A. Sheikholeslami, B. Payne, and J. Lin, "Will ADCs overtake binary front-ends in backplane signaling?," presented at the IEEE Int. Solid-State Circuits Conf., San Francisco, CA, 2009, Special Evening Session, SE3.

[9] I. Mehr, P. C. Maulik, and D. Paterson, "A 12-bit integrated analog front end for broadband wireline networks," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 302–309, Mar. 2002.

[10] M. Moyal, M. Groepl, and T. Blon, "A 25-kft, 768-kb/s CMOS Analog front end for multiple-bit-rate DSL transceiver," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1961–1972, Dec. 1999.

[11] M. Bathaee, H. Ghezelayagh, W. Q. Heng, D. Nicolae, O. Fratu, R. Pop, G. Dilimot, V. Feies, P. Agache, R. Ruscu, M. lorgulescu, J. Gang, W. M. Lin, M. Lei, D. Z. Hui, and W. Tao, "A 0.13µm CMOS SoC for all format blue and red laser DVD front-end digital signal processor," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf. (ISSCC 2006)*, pp. 1012–1021

[12] K. JooSeon, C. GoangSeog, P. HyunJeong, A.YoungJun, K. MyungSik, C. KiSun, L. TaeHo, H. MyungHee, B. JumHan, P. HyunSoo, L. YoonWoo, J. SooYul, S. JoongEon, and S. DongHo, "A0.18µm CMOS SoC of a front-end hardware platform for DVD- Multi recorders," in *Dig. Tech. Papers Int. Conf. Consum. Electron. (ICCE 2005)*, pp. 53–54.

[13] H. Runsheng, N. Nazari, and S. Sutardja, "A DSP based receiver For 1000 BASE-T PHY," in *Dig. Tech. Papers Solid-State Circuits Conf. (ISSCC 2001)*, p. 458.

[14] H.-P. Lin, N. F. Chen, J.-T. Lai, and A.-Y.Wu, "1000 BASE-T Gigabit Ethernet baseband DSP IC design," in *Proc. 2004 Int. Symp. CircuitsSyst. (ISCAS '04)*, vol. 4, pp. IV-401–IV-404.

[15] B. S. Leibowitz, J. Kizer, H. Lee, F. Chen, A. Ho, M. Jeeradit, A. Bansal, T. Greer, S. Li, R. Farjad-Rad, W. Stonecypher, Y. Frans, B. Daly, F. Heaton, B. W. Gariepp, C. W. Werner, N. Nguyen, V. Stojanovic, and J. L. Zerbe, "A 7.5 Gb/s 10-Tap DFE receiver with first Tap partial response, spectrally gated adaptation, and 2nd- Order data-filtered CDR," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf. (ISSCC 2007)*, pp. 228–599.

[16] J. F. Bulzacchelli, M. Meghelli, S. V. Rylov, W. Rhee,
A.V Rylyakov, H. A. Ainspan, B. D. Parker,M. P. Beakes, C. Aichin, T. J. Beukema, P.K. Pepeljugoski, L. Shan, Y. H. Kwark, S. Gowda, and D. J. Friedman, "A 10-Gb/s 5-Tap DFE/4-Tap FFE transceiver in 90-nm CMOS technology,"*IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2885–2900, Dec. 2006.

[17] Henk Jan Bergveld, Kees M. M. van Kaam, Domin M.W. "A Low- Power Highly Digitized Receiver for 2.4-GHz-Band GFSK Applications", IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, VOL. 53, NO. 2, FEBRUARY 2005.

[18] E-Hung Chen, Ramy Yousry, Tamer Ali, and Chih-Kong Ken Yang "10Gb/s Serial I/O Receiver Based on Variable
Reference ADC", Symposium on VLSI Circuits Digest of
Technical Papers 2011

[19] Jun Cao et al, "A 500mW digitally calibrated AFE in 65nm CMOS for 10Gb/s Serial links over backplane and multimode fiber,"*ISSCC* 2009, pp.370-371.

[20] E-Hung Chen et al, "Adaptation of CDR and full scale range of ADC-based SerDes receiver," *VLSI* 2009, pp.12-13.

[21] Ayman Shafik, Keytaek Lee, Ehsan Zhian Tabasy, and SamuelPalermo, "Embedded Equalization for ADC-Based Serial I/OReceivers", 2011 IEEE.

[22] J. Cao *et al.*, "A 500 mW ADC-based CMOS AFE with digital calibration for 10 Gb/s serial links over KR- backplane and multimode fiber," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp.1172-1185, June 2010.

[23] P. Schvan *et al.*, "A 24GS/s 6b ADC in 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 544-634, Feb. 2008